CLAIMS:

1. An electronic memory component or memory module (100), having at least one memory cell area (10) in which physical states (P) representing regular data are mapped by means of at least one mapping function (A) that describes at least one error correction code, for example at least one Hamming code, characterized by at least one further physical state representing at least one exceptional or special state (L, S) in the error correction code.

2. A memory component or memory module as claimed in Claim 1, characterized in that the error correction code and/or the possible reactions to the various physical states are implemented using hardware and/or software.

3. A memory component or memory module as claimed in Claim 1 or 2, characterized in that the exceptional or special state (L, S) in the error correction code is given

- by the flow of leakage currents while memory cell transistors of any one bit are switched off;
- as a memory block or memory cell area (10) which has not yet been written;
- by manipulating the memory cell area (10), for example by irradiating the memory cell area (10) with electromagnetic particles or waves; and/or
- by the erasure of a memory block or memory cell area (10).

4. A memory component or memory module as claimed in at least one of Claims 1 to 3, characterized

- in that the error correction code is configured as at least one Hamming code, which is designed for correcting one-bit errors in the memory cell area (10) and has a Hamming distance of 3, so that each valid code word or data word differs from any other code word or data word in at least three bits, and
- in that for each eight-bit code word or data word (D: D0, D1, D2, D3, D4, D5, D6, D7), additionally at least four redundant bits (R: R0, R1, R2, R3) are provided, resulting in twelve-bit code words or data words.

5. A memory component or memory module as claimed in Claim 4, characterized in that the Hamming code is designed such that each valid twelve-bit code word or data word has

- at least two set bits (= "1") and/or
- at least two erased bits (= "0"),
- so that each valid twelve-bit code word or data word has a minimum Hamming distance of 2 for special states
- in which all bits of a byte are set (= "1") (Z1) or
- in which all bits of a byte are erased (= "0") (Z0).

6. A memory component or memory module as claimed in Claim 4 or 5, characterized in that the four redundant bits (R: R0, R1, R2, R3)

- in the test mode (T), which also comprises states in which all bits of a byte are set (= "1") (Z1) or in which all bits of a byte are erased (= "0") (Z0), are selected as follows:

-- third redundant bit (R3) corresponds to parity of the seventh data bit (D7),
of the sixth data bit (D6),
of the fifth data bit (D5),
of the fourth data bit (D4),
of the first data bit (D1);

-- second redundant bit (R2) corresponds to parity of the seventh data bit (D7),
of the sixth data bit (D6),
of the third data bit (D3),
of the second data bit (D2),
of the zero data bit (D0);

-- first redundant bit (R1) corresponds to parity of the seventh data bit (D7),
of the fifth data bit (D5),
of the fourth data bit (D4),
of the third data bit (D3),
of the zero data bit (D0);

-- zero redundant bit (R0) corresponds to parity of the sixth data bit (D6),
of the fourth data bit (D4),
of the third data bit (D3),

of the second data bit (D2),
of the first data bit (D1);

and/or

- in the normal mode (N) are selected as follows:

-- third redundant bit (R3) corresponds to negated parity
of the seventh data bit (D7),
of the sixth data bit (D6),
of the fifth data bit (D5),
of the fourth data bit (D4),
of the first data bit (D1);

-- second redundant bit (R2) corresponds to negated parity
of the seventh data bit (D7),
of the sixth data bit (D6),
of the third data bit (D3),
of the second data bit (D2),
of the zero data bit (D0);

-- first redundant bit (R1) corresponds to negated parity
of the seventh data bit (D7),
of the fifth data bit (D5),
of the fourth data bit (D4),
of the third data bit (D3),
of the zero data bit (D0);

-- zero redundant bit (R0) corresponds to negated parity
of the sixth data bit (D6),
of the fourth data bit (D4),
of the third data bit (D3),
of the second data bit (D2),
of the first data bit (D1).

7. A memory component or memory module as claimed in at least one of Claims 4 to 6, characterized in that the data bits (D: D0, D1, D2, D3, D4, D5, D6, D7) and the redundant bits (R: R0, R1, R2, R3) together correspond to the physical states (P).

8. A memory component or memory module as claimed in at least one of Claims 1 to 7, characterized in that the memory cell matrix (1) is assigned

- at least one source (12a, 12b),
- at least one bit line (14),
- at least one word line (16) and
- at least one control gate (18).

9. A memory component or memory module as claimed in at least one of Claims 1 to 8, characterized in that the memory component or memory module (100) is configured

- as an E[rasable]P[rogrammable]R[ead]O[nly]M[emory],
- as an E[lectrically]E[rasable]P[rogrammable]R[ead]O[nly]M[emory],
- as a Flash memory,
- as a R[ead]O[nly]M[emory] or
- as a R[andom]A[ccess]M[emory].

10. The use of at least one electronic memory component or memory module (100) as claimed in at least one of Claims 1 to 9 in order to detect and/or label invalid physical states or physical states that are special in some other way.

11. A method of operating at least one electronic memory component or memory module, in particular as claimed in at least one of Claims 1 to 9, in which physical states (P) representing regular data are mapped by means of at least one mapping function (A) that describes at least one error correction code, for example at least one Hamming code, characterized in that at least one further physical state in the form of at least one exceptional or special state (L, S) in the error correction code can be detected, encoded and/or indicated by means of the mapping function (A).

12. A method as claimed in Claim 11, characterized in that the further physical state can be detected, encoded and/or indicated on the basis of its bit pattern, even in the case of an error detection and/or correction operation which can be used only to a limited extent for the regular data.

13. A method as claimed in Claim 11 or 12, characterized by at least one redundant data encoding operation.

14. A method as claimed in at least one of Claims 11 to 13, characterized

- in that at least one Hamming code intended for correcting one-bit errors in the memory cell area (10) and having a Hamming distance of 3 is selected as the error correction code, so that each valid code word or data word differs from any other code word or data word in at least three bits, and

- in that for each eight-bit code word or data word (D: D0, D1, D2, D3, D4, D5, D6, D7), additionally at least four redundant bits (R: R0, R1, R2, R3) are provided, so that twelve-bit code words or data words are formed.

15. A method as claimed in Claim 14, characterized in that the Hamming code is selected such that each valid twelve-bit code word or data word has

- at least two set bits (= "1") and/or

- at least two erased bits (= "0"),

- so that each valid twelve-bit code word or data word has a minimum Hamming distance of 2 for special states

- in which all bits of a byte are set (= "1") (Z1) or

- in which all bits of a byte are erased (= "0") (Z0).

16. A method as claimed in Claim 14 or 15, characterized

- by at least one twelve-fold "and" operation to which the data bits (D: D0, D1, D2, D3, D4, D5, D6, D7) and the redundant bits (R: R0, R1, R2, R3) can be applied and/or

- by at least one twelve-fold "nor" operation to which the data bits (D: D0, D1, D2, D3, D4, D5, D6, D7) and the redundant bits (R: R0, R1, R2, R3) can be applied

- for detecting the exceptional or special state (L, S) in the error correction code.

17. A method as claimed in at least one of Claims 14 to 16, characterized in that the four redundant bits (R: R0, R1, R2, R3)

- in the test mode (T), which also comprises states in which all bits of a byte are set (= "1") (Z1) or in which all bits of a byte are erased (= "0") (Z0), are selected as follows:

-- third redundant bit (R3) corresponds to parity of the seventh data bit (D7), of the sixth data bit (D6),

of the fifth data bit (D5),
of the fourth data bit (D4),
of the first data bit (D1);

-- second redundant bit (R2) corresponds to parity of the seventh data bit (D7),
of the sixth data bit (D6),
of the third data bit (D3),
of the second data bit (D2),
of the zero data bit (D0);

-- first redundant bit (R1) corresponds to parity of the seventh data bit (D7),
of the fifth data bit (D5),
of the fourth data bit (D4),
of the third data bit (D3),
of the zero data bit (D0);

-- zero redundant bit (R0) corresponds to parity of the sixth data bit (D6),
of the fourth data bit (D4),
of the third data bit (D3),
of the second data bit (D2),
of the first data bit (D1);

and/or

- in the normal mode (N) are selected as follows:

-- third redundant bit (R3) corresponds to negated parity
of the seventh data bit (D7),
of the sixth data bit (D6),
of the fifth data bit (D5),
of the fourth data bit (D4),
of the first data bit (D1);

-- second redundant bit (R2) corresponds to negated parity
of the seventh data bit (D7),
of the sixth data bit (D6),
of the third data bit (D3),
of the second data bit (D2),
of the zero data bit (D0);

-- first redundant bit (R1) corresponds to negated parity
of the seventh data bit (D7),

of the fifth data bit (D5),
of the fourth data bit (D4),
of the third data bit (D3),
of the zero data bit (D0);

-- zero redundant bit (R0) corresponds to negated parity
of the sixth data bit (D6),
of the fourth data bit (D4),
of the third data bit (D3),
of the second data bit (D2),
of the first data bit (D1).

18. A method as claimed in at least one of Claims 14 to 17, characterized in that the data bits (D: D0, D1, D2, D3, D4, D5, D6, D7) and the redundant bits (R: R0, R1, R2, R3) together correspond to the physical states (P).

19. An error correction circuit (200), implemented or integrated in at least one electronic memory component or memory module (100) as claimed in at least one of Claims 1 to 9 and/or operating in accordance with the method as claimed in at least one of Claims 11 to 18.

20. An error correction circuit as claimed in Claim 19, characterized by at least one computation unit (C) which is provided for computing or determining redundant bits (R: R0, R1, R2, R3), at least one multiplexing unit (M)

- to which noninverted redundant bits can be applied in the test mode (T) and/or
- to which inverted redundant bits can be applied in the normal mode (N)

being connected downstream of said computation unit (C).

21. An error correction circuit as claimed in Claim 19 or 20, characterized

- by at least one twelve-fold "and" gate (G1) to which the data bits (D: D0, D1, D2, D3, D4, D5, D6, D7) and the redundant bits (R: R0, R1, R2, R3) can be applied and/or
- by at least one twelve-fold "nor" gate (G0) to which the data bits (D: D0, D1, D2, D3, D4, D5, D6, D7) and the redundant bits (R: R0, R1, R2, R3) can be applied

for detecting the exceptional or special state (L, S) in the error correction code.

22. An error correction circuit as claimed in at least one of Claims 19 to 21, characterized by at least one multiplexing unit (M) to which the redundant bits (R: R0, R1, R2, R3) can be applied, which multiplexing unit is provided for switching

- in the test mode (T), the nonnegated redundant bits and/or
- in the normal mode (N), the negated redundant bits

through to at least one correction unit (U) connected downstream of the multiplexing unit (M).

23. An error correction circuit as claimed in Claim 20 or 22, characterized by at least one inverter unit (I) connected upstream of that input (EN) of the multiplexing unit (M) which is provided for the normal mode (N).

24. An error correction circuit as claimed in Claim 22 or 23, characterized in that the correction unit (U) computes and/or determines the expected redundant bits from the data bits (D: D0, D1, D2, D3, D4, D5, D6, D7), and compares these expected redundant bits with the redundant bits (R: R0, R1, R2, R3) switched through by the multiplexing unit (M), said redundant bits (R: R0, R1, R2, R3) being nonnegated in the test mode (T) and negated in the normal mode (N).

25. The use of the method as claimed in at least one of Claims 11 to 18 in order to implement at least one additional safety feature in at least one smart card, in particular in at least one smart card controller unit.